UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/771,749	02/03/2004	Hyoung-Sub Kim	8750-063	3653

20575 7590 02/21/2006

MARGER JOHNSON & MCCOLLOM, P.C.
210 SW MORRISON STREET, SUITE 400
PORTLAND, OR 97204

EXAMINER	
CAO, PHAT X	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/771,749	KIM, HYOUNG-SUB	
	Examiner	Art Unit	
	Phat X. Cao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-13* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The cancellation of claims 14-20 in Paper filed on 12/6/05 is acknowledged.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 4, 8-10 and 12 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohkawa (US. 6,091,154).

Regarding claims 1, 8 and 9, Ohkawa (Fig. 19C) discloses a semiconductor device comprising: a semiconductor substrate 40 having a cell array region and a peripheral circuit region (column 23, lines 35-39); a plurality of word line patterns placed on the cell array region, the word line patterns including a word line 48 and a word line cap layer (not shown in Fig. 19C, see column 23, lines 13-23, and word line cap layer 7b shown in Fig. 13A); a gate pattern 48 placed on the peripheral circuit region; an interlayer insulating layer 63 of BPSG (column 23, lines 30-31) covering an upper surface of the semiconductor substrate 40 having the word line patterns and the gate pattern 48; a self-aligned contact spacer 66 covering a sidewall of the self-aligned contact hole; and gate spacers 60 on sidewalls of the gate pattern 48 being disposed entirely between sidewalls of the gate pattern 48 and the interlayer insulating layer 63, a width of the gate spacers 60 of 50 to 200 nm (column 23, lines 12-14) being

substantially different and greater than from a width of the self-aligned contact spacer 66 of 30 to 100 nm (column 23, lines 1-3).

Regarding claims 2 and 10, Ohkawa (Fig. 19C) further discloses the word line spacers 60 interposed between sidewalls of the word line patterns 48 placed opposite to the self-aligned contact hole 64 and the interlayer insulating layer 63, the word line spacers 60 being formed of the same material layer as the gate spacers 60, the word line spacers 60 having the same width as that of the gate spacers 60 (column 23, lines 17-20).

Regarding claims 4 and 12, Ohkawa (Fig. 19C) further discloses a contact etch stop layer (61,62) disposed in contact with the word line spacers 60 and the interlayer insulating layer 63 in the cell array region, and disposed in contact with the gate spacers 60 and the interlayer insulating layer 63 in the peripheral circuit region.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohkawa (US. 6,091,154) in view of Chang et al (US. 5,817,562).

Regarding claim 11, Ohkawa does not disclose a spacer etch stop layer as claimed.

However, Chang (Fig. 5) teaches the forming of a spacer etch stop layer 24 between the word line spacer 26 and one of the two word line patterns 16, between the gate spacer 26 and the gate pattern 16, and between the self-aligned contact spacer 28 and the two word line patterns 16. Accordingly, it would have been obvious to modify the device of Ohkawa by forming a spacer etch stop layer with the structures as set forth above because such forming a structure of spacer etch stop layer would stop the etching through the substrate during the forming of the sidewall spacers 26, as taught by Chang (see Fig. 4 and column 6, lines 17-25).

Regarding claim 5, Ohkawa's Fig. 19C discloses that the interlayer insulating layer 63 is a BPSG layer (column 23, lines 30-34), but not a PSG layer.

However, in the alternative embodiment (Fig. 1), Ohkawa teaches that the BPSG interlayer insulating layer may be replaced by a PSG interlayer insulating layer (column 8, lines 12-14). Accordingly, it would have been obvious to use BPSG or PSG as the material for the interlayer insulating layer because they both provide an equivalent in function as an insulating material, as taught by Ohkawa.

5. Claims 6-7 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohkawa (US. 6,091,154) in view of Kim et al (US. 6,649,503).

Ohkawa does not disclose that the self-aligned contact hole 64 having a diameter of the upper contact hole greater than a diameter of the lower contact hole.

However, Kim (Fig. 7A) teaches the forming of a self-aligned contact hole 230 having a diameter of the upper contact hole greater than the lower contact hole (column 6, lines 7-16), and a self-aligned contact spacer 250 covering a side wall of the self-

aligned contact hole 230. Accordingly, it would have been obvious to modify the self-aligned contact hole 64 of Ohkawa by forming the upper contact hole having a diameter greater than a diameter of the lower contact hole because such a self-aligned contact hole structure would provide a contact plug having a wide width at the upper portion and a narrow width at a lower portion, as taught by Kim (see Fig. 8A and column 6, lines 7-16).

Allowable Subject Matter

6. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose a spacer etch stop layer structure as recited in the amended claim.

Response to Arguments

7. Regarding claim 1, Applicant argues that Ohkawa does not teach the word line pattern 48 includes a word line and a word line capping layer as claimed.

This argument is not persuasive because Ohkawa (Fig. 19C) does teach a word line pattern including a word line 48 and a word line cap layer (not shown in Fig. 19C, see column 23, lines 13-23, and a word line cap layer 7b shown in Fig. 13A).

Regarding claim 2, Applicant argues that in Ohkawa's Fig. 19C, the width of the word line spacer 60 in the memory cell region is not substantially the same as a width of the gate spacer 60 in the peripheral circuit region.

This argument is not persuasive because Ohkawa clearly teaches that the word line spacers 60 in the memory cell portion and the gate spacers 60 in the peripheral circuit portion are formed by depositing and etching an HTO film having a thickness of 50 to 150 nm formed over the substrate whole surface (see Fig. 19A and column 23, lines 17-20). Therefore, both word line spacers 60 and gate spacers 60 would have the same maximum width of 50 to 150 nm.

Regarding claim 4, Applicant argues that Ohkawa's Fig. 19C does not teach the contact etch stop layer as amended.

This argument is not persuasive because if the combination of two layers 61 and 62 is interpreted as "a contact etch stop layer", then Ohkawa does suggest the invention as claimed. Specifically, Ohkawa's Fig. 19C teaches a contact etch stop layer (61,62) disposed in contact with the word line spacers 60 and the interlayer insulating layer 63 in the cell array region, and disposed in contact with the gate spacers 60 and the interlayer insulating layer 63 in the peripheral circuit region.

Regarding claim 5, Applicant argues that Ohkawa fails to teach the interlayer insulating layer 63 having a material as claimed.

This argument is not persuasive because Ohkawa clearly teaches that the interlayer insulating layer 63 can be made by claimed material such as BPSG or PSG (column 8, lines 12-14).

Regarding claims 6-7, in response to Applicant's arguments, the new reference is applied in the new ground of rejection to show the obviousness of the invention as claimed.

Regarding claims 9 and 11, Applicant argues that the gate spacer 60 of Ohkawa is not disposed entirely between a sidewall of a gate pattern and the inter-insulation layer.

This argument is not persuasive because if only a portion of the dielectric layer 60 formed on a sidewall of the gate pattern 48 is considered as a gate spacer, then clearly, the gate spacer formed on a sidewall of the gate pattern 48 is disposed entirely between a sidewall of the gate pattern 48 and the inter-layer insulating layer 63.

Regarding amended claim 3, Applicant's argument is persuasive. Therefore, claim 3 is allowed.

The rest of Applicant's arguments are considered in view of the ground rejection above.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is 571-272-1703. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on 571-272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC
February 17, 2006

PHAT X. CAO
PRIMARY EXAMINER